Abstract

1   A time division multiplex data recovery system using a closed-loop phase lock loop

2   (PLL) and delay locked loop (DLL) is disclosed. In other words, one closed loop comprises both

3   a phase locked loop (PLL) and a delay locked loop (DLL) in a novel time division multiplex data

4   recovery system. This new architecture comprises a 4 stage Voltage Controlled Oscillator (VCO)

5   used to generate 8 clock signals, 45 degrees phase shifted from one another, for 8 receivers to do

6   the oversampling. An interpolator tracks the received data signal and feeds it back to the

7   Phase/Frequency Detector (PFD). The PFD has a second input of the reference clock which the

8   PFD uses along with the interpolator input to correct the frequency of the PLL. The PLL operates

9   at a high bandwidth. The DLL's bandwidth is several orders lower than the PLL. The DLL

10   activates only a multiplexer and an interpolator continuously, thereby drawing a minimum

11   amount of power.